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DESIGNING AND ANALYSIS MULTI-LEVEL INVERTER CAPABLE OF POWER FACTOR CONTROL WITH DC LINK SWITCHES

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ABSTRACT: A multilevel inverter for generating 17 voltage levels using a three-level flying capacitor inverter and cascaded H-bridge modules with floating capacitors has been proposed. Various aspects of the proposed inverter like capacitor voltage balancing have been presented in the present paper. Experimental results are presented to study the performance of the proposed converter. The stability of the capacitor balancing algorithm has been verified both during transients and steady-state operation. All the capacitors in this circuit can be balanced instantaneously by using one of the pole voltage combinations. Another advantage of this topology is its ability to generate all the voltages from a single dc-link power supply which enables back-to-back operation of converter. Also, the proposed inverter can be operated at all Load. Additional advantage is, if one of the H-bridges fail, the inverter can still be operated at full load with reduced number of levels. This configuration has very low dv/dt and common-mode voltage variation.

1. Introduction

WITH the advent of multilevel inverters, the performance of medium and high-voltage drives have changed drastically As the number of voltage levels increases, the output voltage is closer to sine wave with reduced harmonic content, improving the performance of the drive greatly as presented in [4] and [5]. One of the pioneering works in the field of multilevel inverters is the neutral point clamped inverter [6]. On the other hand, the use of multiple isolated dc sources using H-bridges for plasma stabilization generating multiple voltage levels was presented in [7]. The work presented in [8] analyzes the issues with the scheme of cascading multiple rectifiers and proposes a solution for

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balancing the capacitors. The work presented in [9] generates multiple voltage levels by switching the load current through capacitors. Here, the voltage through the capacitors can be maintained at desired value by changing the direction of load current through the capacitor by choosing the redundant states for the same pole voltage. The work presented in [10] combines the concepts of work presented in [9] and [7].

` Here, the floating capacitor H-bridges are used to generate multiple output voltages. The voltages of the capacitors are maintained at their intended values by switching through redundant states for the same voltage level. The works presented in [11]–[15] address aspects of using cascaded H-bridges and propose various efficient control algorithms. Modular multilevel converters which are very popular in HVDC applications are another genre of multilevel converters which can be used for motor drive applications as presented in [16]–[18]. The concept of cascading flying capacitor inverter with neutral point clamped inverter is presented in [19]. Similar concept has been made available commercially as ABB ACS 2000. The concept of increasing the number of levels using flying capacitor inverter with cross connected capacitors has been presented in [20]. An interesting configuration to generate 17 voltage levels using multiple capacitors is presented in [21]. However in [20] and [21], the capacitor voltages cannot be balanced instantaneously.

They can be balanced only at the fundamental frequency. A single-phase seventeen-level inverter configuration is presented in [22] uses large number of power supplies and has a floating load. This is more suitable for STATCOM applications. An attractive algorithm for operating seventeen level inverter has been presented in [23]. In the present paper, we propose a new 17-level inverter formed by cascading three-level flying capacitor inverter with floating capacitor H-bridges which uses a single dc supply and derives all the required voltage levels from it. The performance of the proposed configuration is experimentally verified both for steady state operation and during transients and the results are presented.

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2. Proposed Circuit Operation

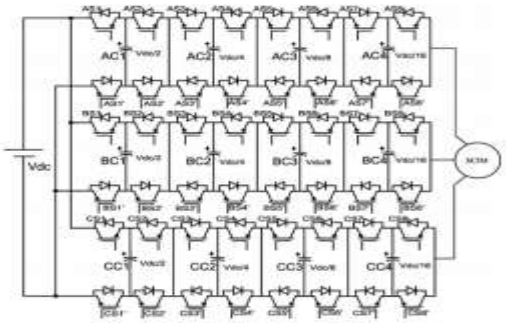

Fig. 1. Three-phase power schematic of the proposed seventeen-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

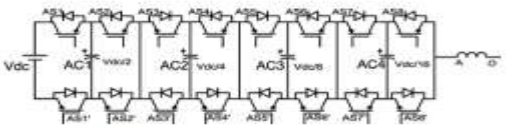

Fig. 2. One phase of the proposed 17-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

The proposed converter is a hybrid multilevel topology employing a three-level flying capacitor inverter and cascading it with three floating capacitor H-Bridges. The three-phase power schematic is shown in Fig. 1. The voltages of capacitors AC1, BC1, and CC1 are maintained at Vdc/2. Capacitors AC2, BC2, and CC2 are maintained at voltage level of Vdc/4. Similarly capacitors AC3, BC3, and CC3 are maintained at voltage level of Vdc/8 and capacitors AC4, BC4, and CC4 are maintained at voltage level of Vdc/16. Each cascaded H-bridge can either add or subtract its voltage to the voltage generated by its previous stage. In addition to that, the CHBs can also be bypassed. The resulting inverter pole voltage is the arithmetic sum of voltages of each stage. The schematic diagram for one phase of the proposed converter is shown in Fig. 2. The switch pairs (AS1, AS1'), (AS2, AS2'), (AS3, AS3'), (AS4, AS4'), (AS5, AS5'), (AS6, AS6'), (AS7, AS7'), and (AS8, AS8') are switched in complementary fashion with appropriate dead time. Each switch pair has two distinct logic states, namely top device is ON (denoted by 1) or the bottom device is ON (denoted by 0). Therefore, there are 256 (28) distinct switching combinations possible. Each voltage level can be generated using one or more switching states (pole voltage redundancies). By switching through the redundant switching combinations (for the same pole voltage), the current through capacitors can be reversed and their voltages can be controlled to their prescribed values. This method of balancing the capacitor voltages at all load currents and power factors instantaneously has been observed for 17 pole voltage levels. They are 0, Vdc/16, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2,

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9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc. However, by switching through all the possible pole voltage switching combinations, 31 distinct pole voltage levels can be generated using the proposed topology. In the additional 14 levels, the voltages of capacitors can be balanced only in a fundamental cycle.

3. Pole Voltage Redundancies

There are 82 switching combinations (see Table I) that can be used to generate the above mentioned 17 pole voltage levels where instantaneous capacitor voltage balancing is possible. The effect of 82 switching combinations on every capacitor's charge state (charge or discharge) for positive direction of current (i.e., when the pole is sourcing current as is shown in Table I.

S. No.	Pole Voltage	Switch State (S1, S2, S3, S4, S5, S6, S7, S8)	C1*	C2*	C3*	C4*
1	0	(0, 0, 0, 0, 0, 0, 0, 0)	0	0	0	0
2	Vdc/16	(0, 0, 0, 0, 0, 0, 0, 1)	0	0	0	–
3		(0, 0, 0, 0, 0, 1, 1, 0)	0	0	–	+
4		(0, 0, 0, 1, 1, 0, 1, 0)	0	–	+	+
5		(0, 1, 1, 0, 1, 0, 1, 0)	–	+	+	+
6		(1, 0, 1, 0, 1, 0, 1, 0)	+	+	+	+
7	Vdc/8	(0, 0, 0, 0, 0, 1, 0, 0)	0	0	–	0
8		(0, 0, 0, 1, 1, 0, 0, 0)	0	–	+	0
9		(0, 1, 1, 0, 1, 0, 0, 0)	–	+	+	0
10		(1, 0, 1, 0, 1, 0, 0, 0)	+	+	+	0
11	3 Vdc/16	(0, 0, 0, 0, 0, 1, 0, 1)	0	0	–	–
12		(0, 0, 0, 1, 0, 0, 1, 0)	0	–	0	+
13		(0, 0, 0, 1, 1, 0, 0, 1)	0	–	+	–
14		(0, 1, 1, 0, 0, 0, 1, 0)	–	+	0	+
15		(0, 1, 1, 0, 1, 0, 0, 1)	–	+	+	–
16		(1, 0, 1, 0, 0, 0, 1, 0)	+	+	0	+
17		(1, 0, 1, 0, 1, 0, 0, 1)	+	+	+	–
18	Vdc/4	(0, 0, 0, 1, 0, 0, 0, 0)	0	–	0	0
19		(0, 1, 1, 0, 0, 0, 0, 0)	–	+	0	0
20		(1, 0, 1, 0, 0, 0, 0, 0)	+	+	0	0
21	5 Vdc/16	(0, 0, 0, 1, 0, 0, 0, 1)	0	–	0	–
22		(0, 0, 0, 1, 0, 1, 1, 0)	0	–	–	+
23		(0, 1, 0, 0, 1, 0, 1, 0)	–	0	+	+
24		(0, 1, 1, 0, 0, 0, 0, 1)	–	+	0	–
25		(0, 1, 1, 0, 0, 1, 1, 0)	–	+	–	+
26		(1, 0, 0, 0, 1, 0, 1, 0)	+	0	+	+
27		(1, 0, 1, 0, 0, 0, 0, 1)	+	+	0	–
28		(1, 0, 1, 0, 0, 1, 1, 0)	+	+	–	+
29	3 Vdc/8	(0, 0, 0, 1, 0, 1, 0, 0)	0	–	–	0
30		(0, 1, 0, 0, 1, 0, 0, 0)	–	0	+	0
31		(0, 1, 1, 0, 0, 1, 0, 0)	–	+	–	0
32		(1, 0, 0, 0, 1, 0, 0, 0)	+	0	+	0
33		(1, 0, 1, 0, 0, 1, 0, 0)	+	+	–	0
34	7 Vdc/16	(0, 0, 0, 1, 0, 1, 0, 1)	0	–	–	–
35		(0, 1, 0, 0, 0, 0, 1, 0)	–	0	0	+
36		(0, 1, 0, 0, 1, 0, 0, 1)	–	0	+	–
37		(0, 1, 1, 0, 0, 1, 0, 1)	–	+	–	–
38		(1, 0, 0, 0, 0, 0, 1, 0)	+	0	0	+
39		(1, 0, 0, 0, 1, 0, 0, 1)	+	0	+	–
40		(1, 0, 1, 0, 0, 1, 0, 1)	+	+	–	–
41	Vdc/2	(0, 1, 0, 0, 0, 0, 0, 0)	–	0	0	0
42	Vdc/2	(1, 0, 0, 0, 0, 0, 0, 0)	+	0	0	0
43	9 Vdc/16	(0, 1, 0, 0, 0, 0, 0, 1)	–	0	0	–
44		(0, 1, 0, 0, 0, 1, 1, 0)	–	0	–	+
45		(0, 1, 0, 1, 1, 0, 1, 0)	–	–	+	+
46		(1, 0, 0, 0, 0, 0, 0, 1)	+	0	0	–
47		(1, 0, 0, 0, 0, 1, 1, 0)	+	0	–	+
48		(1, 0, 0, 1, 1, 0, 1, 0)	+	–	+	+
49		(1, 1, 1, 0, 1, 0, 1, 0)	0	+	+	+
50	5 Vdc/8	(0, 1, 0, 0, 0, 1, 0, 0)	–	0	–	0
51		(0, 1, 0, 1, 1, 0, 0, 0)	–	–	+	0
52		(1, 0, 0, 0, 0, 1, 0, 0)	+	0	–	0
53		(1, 0, 0, 1, 1, 0,0, 0)	+	–	+	0
54		(1, 1, 1, 0, 1, 0, 0, 0)	0	+	+	0
55	11 Vdc/16	(0, 1, 0, 0, 0, 1,0, 1)	–	0	–	–
56		(0, 1, 0, 1, 0, 0, 1, 0)	–	–	0	+
57		(0, 1, 0, 1, 1, 0, 0, 1)	–	–	+	–
58		(1, 0, 0, 0, 0, 1, 0, 1)	+	0	–	–
59		(1, 0, 0, 1, 0, 0, 1, 0)	+	–	0	+
60		(1, 0, 0, 1, 1, 0, 0, 1)	+	–	+	–
61		(1, 1, 1, 0, 0, 0, 1, 0)	0	+	0	+
62		(1, 1, 1, 0, 1, 0, 0, 1)	0	+	+	–
63	3 Vdc/4	(0, 1, 0, 1, 0, 0, 0, 0)	–	–	0	0
64		(1, 0, 0, 1, 0, 0, 0, 0)	+	–	0	0
65		(1, 1, 1, 0, 0, 0, 0, 0)	0	+	0	0
66	13 Vdc/16	(0, 1, 0, 1, 0, 0, 0, 1)	–	–	0	–
67		(0, 1, 0, 1, 0, 1, 1, 0)	–	–	–	+
68		(1, 0, 0, 1, 0, 0, 0, 1)	+	–	0	–
69		(1, 0, 0, 1, 0, 1, 1, 0)	+	–	–	+
70		(1, 1, 0, 0, 1, 0, 1, 0)	0	0	+	+
71		(1, 1, 1, 0, 0, 0, 0, 1)	0	+	0	–
72		(1, 1, 1, 0, 0, 1, 1, 0)	0	+	–	+
73	7 Vdc/8	(0, 1, 0, 1, 0, 1, 0, 0)	–	–	–	0
74		(1, 0, 0, 1, 0, 1, 0, 0)	+	–	–	0
75		(1, 1, 0, 0, 1, 0, 0, 0)	0	0	+	0
76		(1, 1, 1, 0, 0, 1, 0, 0)	0	+	–	0
77	15 Vdc/16	(0, 1, 0, 1, 0, 1, 0, 1)	–	–	–	–
78		(1, 0, 0, 1, 0, 1, 0, 1)	+	–	–	–
79		(1, 1, 0, 0, 0, 0, 1, 0)	0	0	0	+
80		(1, 1, 0, 0, 1, 0, 0, 1)	0	0	+	–
81		(1, 1, 1, 0, 0, 1, 0, 1)	0	+	–	–
82	Vdc	(1, 1, 0, 0, 0, 0, 0, 0)	0	0	0	0

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Table 1

For negative direction of current, the effect of the switching state on the capacitor is reversed. For example, when the controller demands a pole voltage of Vdc/16, there are five different redundant switching combinations to generate it. Each switching combination has a different effect on the state of charge of the capacitors. When the switching state (0, 0, 0, 0, 0, 0, 0, 1) (see Table I) is applied, the capacitor C4 discharges when the pole is sourcing current as [see Fig. 3(a)]. To balance the capacitor C4 and to bring its voltage back to the prescribed value (Vdc/16), one of the other four switching combinations is applied Fig. 3(b)–(e). It can be observed that when switching state (0, 0, 0, 0, 0, 1, 1, 0) is applied, the direction of current in the capacitor C4 is reversed [see Fig. 3(b)] and the capacitor C4 charges. However in this process, the capacitor C3 is discharged. If the capacitor C3 needs charging, switching state redundancy of (0, 0, 0, 1, 1, 0, 1, 0) is applied [see Fig. 3(c)] which discharges C2. To charge C2 one of the switching redundancies shown in Fig. 3(d) and (e) is applied based on the state of charge of capacitor C1. If switching state (0, 1, 1, 0, 1, 0, 1, 0) is applied, the capacitor C1 is discharged and this state charges all the other capacitors as shown in Fig. 3(d). Finally, when switching state of (1, 0, 1, 0, 1, 0, 1, 0) is applied, all the four capacitors are charged for positive direction of current as shown in Fig. 3(e). By switching through the redundant pole voltage combinations, it can be observed that the all the capacitors' voltages can be maintained at their prescribed values while generating pole voltage of Vdc/16 for positive direction of current. If all the capacitors need discharging, the capacitor C4 is discharged first and the remaining capacitors can be discharged during subsequent switching cycles when C4 needs to be charged. For negative direction of current, the effect of the capacitor voltages is the opposite. The entire process of capacitor voltage balancing for pole voltage of Vdc/16 that has been explained is illustrated in Fig. 4. Here, the capacitor voltage variation with application of various redundant states for pole voltage of Vdc/16 has been shown for positive

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direction of current. For other pole voltages namely, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc, a similar strategy can be used to balance all the capacitor voltages. The switching frequency of any CHB module is at most the PWM switching frequency of the converter. This is due to the synchronization of application of the switching state with every PWM transition (the switching state is latched till the next PWM transition). Moreover in this scheme, only the capacitors that contribute to the output pole voltages are switched.

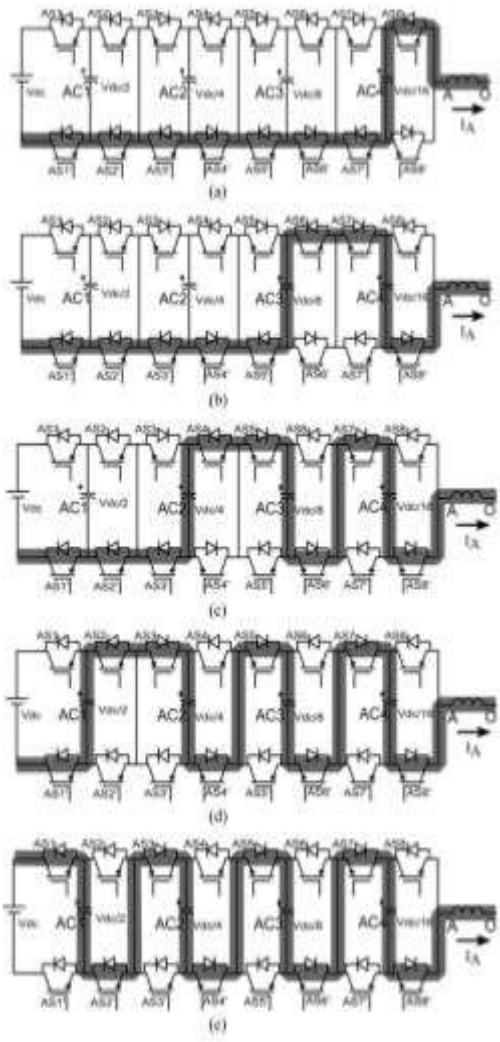

Fig. 3. Switching Redundancies for pole voltage of Vdc/16. (a) Current path for switching state (0, 0, 0, 0, 0, 0, 0, 1). (b) Current path for switching state (0, 0, 0, 0, 0, 1, 1, 0). (c) Current path for switching state (0, 0, 0, 1, 1, 0, 1, 0). (d) Current path for switching state (0, 1, 1, 0, 1, 0, 1, 0). (e) Current path for switching state (1, 0, 1, 0, 1, 0, 1, 0).

4. Simulation Result

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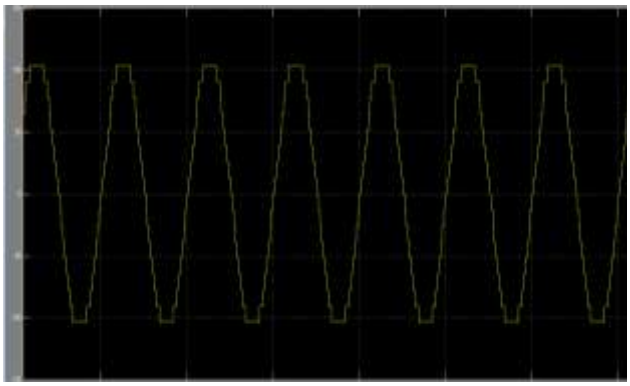

Fig4: Input voltage

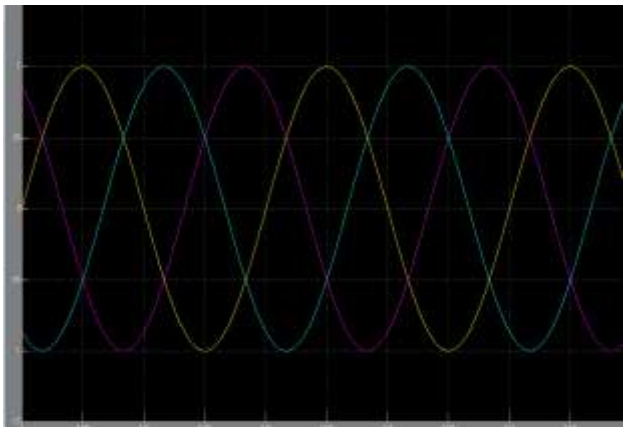

Fig5: Output voltage

5. Conclusion

A new17-level inverter configuration formed by cascading a three-level flying capacitor and three floating capacitor H bridges has been proposed for the first time. The voltages of each of the capacitors are controlled instantaneously in few switching cycles at all loads and power factors obtaining high performance output voltages and currents. The proposed configuration uses a single dc link and derives the other voltage levels from it. This enables back-to-back converter operation where power can be drawn and supplied to the grid at prescribed power factor. Also, the proposed 17-level inverter has improved reliability. In case of failure of one of the H-bridges, the inverter can still be operated with reduced number of levels supplying full power to the load. This feature enables it to be used in critical applications like marine propulsion and traction where reliability is of highest concern. Another advantage of the proposed configuration is modularity and symmetry in structure which enables the inverter to be extended to more number of phases like five-phase and six-phase configurations with the same control scheme. The proposed inverter is analyzed and its performance is experimentally verified for various modulation indices and load currents by running a three-phase 3-kW squirrel cage induction motor. The stability of the capacitor balancing algorithm has been tested experimentally by suddenly accelerating the motor at no load and

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observing the capacitor voltages at various load currents.

6. References

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